Docket No.: 50090-449

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Takashi TERAUCHI, et al.	:	Confirmation Number: 9211
Serial No.: 09/976,341	:	Group Art Unit: 2812
Filed: October 15, 2001	:	Examiner: R.E. Pompey

For: METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE, AND SEMICONDUCTOR DEVICE HAVING MEMORY CELL

TRANSMITTAL OF APPEAL BRIEF

Commissioner for Patents
Washington, DC 20231

Sir:

Submitted herewith in triplicate is Appellant(s) Appeal Brief in support of the Notice of Appeal filed October 2, 2003. Please charge the Appeal Brief fee of $320.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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APPEAL BRIEF

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Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed October 2, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is Mitsubishi Denki Kabushiki Kaisha.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related Appeals and Interferences.

III. STATUS OF CLAIMS

Claims 1 through 20 are pending in this application of which claims 15 through 20 stand

withdrawn from consideration pursuant to the provisions of 37 C.F.R. §1.142(b). Claims 1 through 14 have been finally rejected. It is from the final rejection of claims 1 through 14 that this Appeal is taken.

IV. STATUS OF AMENDMENTS

No Amendment has been filed subsequent to the issuance of the Final Office Action dated July 14, 2003.

V. SUMMARY OF INVENTION

The present invention addresses several problems attendant upon conventional manufacturing methodology (page 2 of the written description of the specification, lines 22 and 23). These problem include deterioration of transistor drive performance due to increased gate interconnection resistance (page 3 of the written description, lines 5 through 7), low yield stemming from defective operation due to bulging silicide films (page 3 of the written description, lines 8 through 24) and reliability issue due to volume expansion of silicide films (paragraph bridging pages 3 and 4 of the written description). The present invention address and solve these problems by providing efficient methodology comprising manipulative steps, which include, inter alia, forming a second silicon film over the entire surface of the substrate covering gate interconnections and then thermally oxidizing the second silicon film to form a thermal oxide with a bird's beak extending into an interface between the gate oxide film and the first silicon film of a gate interconnection, as set forth in independent claims 1 and 6 and schematically illustrated in Fig. 7. In this way, narrowing of gate interconnections is prevented, silicon deficiencies do not arise in the first silicide film and bulging thereof is prevented (page 10 of the written description of the specification, line 23 through page 11, line 20).

The notion of thermally oxidizing a silicon film to form a bird's beak at the interface between

the first silicon film and the gate oxide film is neither disclosed nor suggested by the applied prior art.

VI. ISSUES

A. The Rejection

Claims 1 through 14 were rejected under 35 U.S.C. §103 for obviousness predicated upon Jang in view of Cunningham.

B. The issue which Arises in this Appeal and Requires resolution by the Honorable Board of Patent Appeals and Inferences (the Board) is:

Whether claims 1 through 14 are unpatentable under 35 U.S.C. §103 for obviousness predicated upon Jang in view of Cunningham.

VII. GROUPING OF CLAIMS

The appealed claims do not stand or fall together. Claims 1 through 5 stand or fall together a group with independent claim 1; claims 6 through 14 stand or fall together as a group with independent claim 6.

VIII. ARGUMENT

The Examiner's Position

In the statement of the rejection, the Examiner **admitted** that the method disclosed by Jang falls short of the claimed methods, notably by failing to disclose the step of thermally oxidizing the second silicon film to form a thermal oxide film with a bird's beak extending into the interface between the gate oxide film and first silicon film. Nevertheless, the Examiner concluded that one having ordinary skill in the art would have been motivated to:

> . . . replace the spacers 440 and 460/465 in Jang with the spacers 114 and 120 in Cunningham in order to dictate the offset of the deep source and drain of the MOS device as well as the other reasons indicated above (first full paragraph on page 4 of the July 14, 2003 Final Office Action).

The Examiner is wrong, factually and legally.

Insufficient Facts

The Examiner has **not articulated** the differences between the claimed inventions and Jang. To say that Jang teaches what is claimed except for what is taught by Cunningham does not comply with the legal requirement for **identifying differences** between the claimed invention and the applied reference. *Graham v. John Deere Co.*, 86 S.Ct. 684, 383 U.S. 1, 148 USPQ 459 (1966).

Jang's disclosure lacks considerable more than a suggestion to thermally oxidize the second silicon film to form a thermal oxide with a bird's beak. In fact, it is **impossible** for Jang's thermal oxide film 465 to form a bird's beak which extends into the interface between the gate oxide and silicon film 35, because it is **physically blocked** from reaching it by the thermal oxide 440 which is on the gate structure **and** the intervening polysilicon sidewall spacer 460. Appellant's stress it is **impossible** for the thermal oxide 465 focused upon by the Examiner to get near the interface between the gate oxide and silicon layer 435. This structural difference between the claimed methods and Jang's method is fatal to the imposed rejection under 35 U.S.C. §103.

There is No Motivation

Faced with this formidable difference between the claimed invention and the primary reference, the Examiner concluded that one having ordinary skill in the art would somehow have been led to simply remove Jang's **purposely formed spacers 440 and 460/465** and then replace them with Cunningham's spacers 114 and 120. The reason offered by the Examiner is ". . . to dictate the offset of

the deep source and drain of the MOS device as well as the other reasons indicated above (first full paragraph on page 4 of the July 14, 2003 Office Action). The Examiner is wrong.

In order to establish the requisite realistic motivation, the Examiner must point to a **source** in the applied prior art for **each** claim limitation and to a **source** in the applied prior art for the requisite **motivational** element. *Smiths Industries Medical System v. Vital Signs Inc., 183 F.3d 1347, 51 USPQ2d 1415 (Fed. Cir. 1999).* More to the point, the Examiner is required to make a "thorough and searching" factual inquiry and, based upon that factual inquiry, explain **why** one having ordinary skill in the art would been realistically impelled to modify particular prior art, in this case the particular method disclosed by Jang, to arrive at the claimed invention. *In re Lee, 237 F.3d 1338, 61 USPQ2d 1430, 1433 (Fed. Cir. 2002).* Such a factual inquiry requires clear and particular factual findings as to a specific understanding or specific technological principle which would have realistically impelled one having ordinary skill in the art to modify the particular method disclosed by Jang to arrive at the claimed invention. *Ruiz v. A.B. Chance Co., 234 F.3d 654, 57 USPQ2d 1161 (Fed. Cir. 2000); Ecolochem Inc. v. Southern California Edison, Co. 227 F.3d 1361, 56 USPQ2d 1065 (Fed. Cir. 2000); In re Kotzab, 217 F.3d 1365, 55 USPQ 1313 (Fed. Cir. 2000); In re Dembiczak, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999).* Merely identifying wherein features of a claimed invention are perceived to reside in disparate references does not establish the requisite realistic motivation. *In re Kotzab, supra; Grain Processing Corp. v. American-Maize Products Co., 840 F.2d 902, 5 USPQ2d 1788 (Fed. Cir. 1988).* Rather, a **specific reason** must be offered based upon **facts** to support the asserted motivation--not generalizations. *Ecolochem Inc. v. Southern California Edison, Co. supra; In re Rouffet, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. 1998).*

In applying the above legal tenets to the exigencies of this case, Appellants submit that the requisite realistic motivation element has **not** been established. Specifically, the Examiner's reason "to

dictate the offset of the deep source and drain of the MOS device" does not withstand scrutiny, because Jang has no problem dictating the offset of the source/drain region as apparent from Figs. 4F-4G, noting that source/drain region 480 is formed after forming layers 440, 460 and 465. Thus, Jang has no difficulty dictating the offset of the source/drain regions with layers 440, 460 and 465. That Cunningham may do something else in another context is no reason to dramatically deviate from the expressed teachings of Jang. *In re Lee supra.*

The Examiner also says motivation would stem from ". . . the other reasons indicated above". Applicants hereby question: **What other reasons?** The Examiner's generalization flies in the face of the judicially required factual inquiry for clear and particular factual findings as to a **specific understanding** or **specific technological principle** which would have realistically impelled one having ordinary skill in the art to modify Jang's particular methods to arrive at the claimed invention. *Ruiz v. A.B. Chance Co., supra;); Ecolochem Inc. v. Southern California Edison, Co., supra; In re Kotzab, supra; In re Dembiczak, supra.*

The combined disclosures of Jang and Cunningham does not yield the claimed invention.

Each of independent claims 1 and 6 requires forming the second silicon film **after**, repeat **after**, forming the first diffusion layer. Each of independent claims 1 and 6 requires thermally oxidizing the second silicon film thereafter. But in accordance with the methodology of Cunningham, the polysilicon film is deposited and etched **before**, repeat **before**, forming lightly doped source/drain regions 130a and 130b (column 6 of Cunningham, lines 24 through 34). Accordingly, **if** one having ordinary skill in the art would have been led to modify Jang's methodology by impressing therein the methodology of Cunningham, and that is a big **if** with which Appellants do not agree, the claimed invention would **not** result. *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 USPQ2d 1434

(Fed. Cir. 1988).

Appellants would stress that it is polysilicon layer 460 and silicon oxide layer 465 which the Examiner would propose to strip out of the methodology of Jang. Once these layers are removed, along with layer 440, and replaced with layers 114 and 120 of Cunningham, the resulting method would **not** correspond to that claimed, because the claimed inventions require the manipulative steps of forming the second silicon film **after** forming the first diffusion layer, and thereafter oxidizing. As previously pointed out, the second silicon film would be deposited, the lightly source/drain regions formed and then oxidation would occur according to Cunningham. But that is not what is being claimed. Appellants, therefore, again stress that **if** the applied references are combined, the claimed invention would **not** result. *Uniroyal, Inc. v. Rudkin-Wiley Corp., supra.*

Conclusion

Based upon the foregoing, Appellants submit a *prima facie* basis to deny patentability to the claimed inventions has not been established for lack of the requisite factual basis and want of the requisite realistic motivation. Moreover, even if the applied references are combined as proposed by the Examiner, the claimed inventions would not result. *Uniroyal, Inc. v. Rudkin-Wiley Corp., supra.*

Appellants, therefore, submit that the imposed rejection of claims 1 through 14 under 35 U.S.C. §103 for obviousness predicated upon Jang in view of Cunningham is not factually or legally viable.

IX. PRAYER FOR RELIEF

As argued above, the Examiner's rejection of the appealed claims under 35 U.S.C. §103 is factually and legally erroneous. Appellants, therefore, respectfully solicit the Honorable to reverse the Examiner's rejection of claims 1 through 14 under 35 U.S.C. §103.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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APPENDIX

1. A method of manufacturing a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate;

forming gate interconnections on the gate oxide film, each gate interconnection including a first silicon film, forming an interface with an upper surface of the gate oxide film, and a dielectric film;

forming a first diffusion layer by means of implanting an impurity into the substrate while the gate interconnections are taken as a mask;

forming a second silicon film over the entire surface of the substrate so as to cover the gate interconnections, after formation of the first diffusion layer;

thermally-oxidizing the second silicon film, thereby forming a thermal oxide film with a bird's beak extending into the interface; and

forming an interlayer dielectric film on the thermal oxide film.

2. The method of manufacturing a semiconductor device according to claim 1, wherein each of the gate interconnections includes a silicide film interposed between the first silicon film and the dielectric film.

3. The method of manufacturing a semiconductor device according to claim 1, wherein the first silicon film is a doped silicon film, and

the second silicon film is formed at a temperature higher than 700°C.

4. The method of manufacturing a semiconductor device according to claim 1, wherein the second silicon film is a doped silicon film.

5. The method of manufacturing a semiconductor device according to claim 1, further comprising a step of forming, after formation of the thermal oxide film and prior to formation of the interlayer dielectric film, a second diffusion layer which is higher in impurity concentration than the first diffusion layer, by means of implanting an impurity into the substrate while the thermal oxide film is taken as a mask.

6. A method of manufacturing a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate;

forming gate interconnections on the gate oxide film, each gate interconnection including a first silicon film, forming an interface with an upper surface of the gate oxide film, and a dielectric film;

forming a first diffusion layer by means of implanting an impurity into the substrate while the gate interconnections are taken as a mask;

forming, after formation of the first diffusion layer, a second silicon film over the side surfaces of the first silicon film;

thermally-oxidizing the second silicon film, thereby forming a thermal oxide film with a bird's beak extending into the interface; and

forming, after formation of the thermal oxide film, an interlayer dielectric film over the entire surface of the substrate so as to cover the gate interconnections.

7. The method of manufacturing a semiconductor device according to claim 6, wherein each of the gate interconnections includes a silicide film interposed between the first silicon film and the dielectric film, and

the second silicon film covers side surfaces of the first silicon film and those of the silicide.

8. The method of manufacturing a semiconductor device according to claim 6, wherein the first silicon film is a doped silicon film, and

the second silicon film is formed at a temperature higher than 700°C.

9. The method of manufacturing a semiconductor device according to claim 6, wherein the second silicon film is a doped silicon film.

10. The method of manufacturing a semiconductor device according to claim 6, further comprising a step of forming, after formation of the thermal oxide film and prior to formation of the interlayer dielectric film, a second diffusion layer which is higher in impurity concentration than the first diffusion layer, by means of implanting an impurity into the substrate while the thermal oxide film is taken as a mask.

11. The method of manufacturing a semiconductor device according to claim 6, wherein in the step of thermally-oxidizing the second silicon film, the surface of the second silicon film is thermally-oxided, thereby forming a layer of thermal oxide film and leaving a second silicon film between the layer of the thermal oxide film and the gate interconnections.

12. The method of manufacturing a semiconductor device according to claim 11, wherein on-third to two-thirds of the second silicon film is thermally oxidized, thereby forming the layer of the thermal oxide film.

13. The method of manufacturing a semiconductor device according to claim 1, wherein the

second silicon film is thermally oxidized at a temperature of 700 to 1200°C.

14. The method of manufacturing a semiconductor device according to claim 6, wherein the second silicon film is thermally oxidized at a temperature of 700 to 1200°C.

15. A semiconductor device comprising:

a substrate;

a gate oxide film formed on said substrate;

a plurality of gate interconnections which are formed on said gate oxide film, each of said gate interconnections including a first silicon film and a dielectric film;

an impurity diffusion layer formed in said substrate between said gate interconnections;

a thermal oxide film covering each of said gate electrodes; and

an interlayer dielectric film formed on said thermal oxide film;

wherein a side surface of the dielectric film and a side surface of the first silicon film constitute a single plane.

16. The semiconductor device according to claim 15, wherein each of the gate interconnections includes a silicon film interposed between the first silicon film and the dielectric film, and

a side surface of the dielectric film, a side surface of the first silicon film and a side surface of the silicon film constitute a single plane.

17. The semiconductor device according to claim 16, wherein said thermal oxide film

covers only a side surface of the first silicon film constituting said gate interconnection and a side surface of the silicon film.

18. The semiconductor device according to claim 15, wherein said thermal oxide film covering the side surface of each of said gate interconnections has a uniform thickness.

19. The semiconductor device according to claim 16, wherein said thermal oxide film covering the side surface of the silicide film is thicker than said thermal oxide film covering the side surface of the first silicon film.

20. The semiconductor device according to claim 15, further comprising a second silicon film disposed between the side surface of said gate interconnection and the side surface of said thermal oxide film.